22. (New) A ground plane for a semiconductor chip for mounting on a supporting member in a chip package, comprising:

at least one first capacitor plate provided within the chip, and at least one second capacitor plate, the first and second capacitor plates being separated by a dielectric layer and capacitively coupled to each other via the dielectric layer, and the ground plane comprising at least one first conducting member, including at least one electrically conducting via extending through the supporting member and electrically coupled in series with the second capacitor plate; and wherein

the second capacitor plate comprises a layer of conductive glue.

23. (New) A ground plane according to claim 22, wherein:

a resonant frequency of the capacitance provided by the first capacitor plate and the second capacitor plate, and an inductance provided by the at least one first conducting member, is approximately equal to an intended working frequency of the chip.

24. (New) A ground plane according to claim 22, wherein:

the dielectric layer is an integral part of the chip.

25. (New) A ground plane according to claim 23, wherein:

the dielectric layer is an integral part of the chip.

26. (New) A ground plane according to claim 24, wherein:

the dielectric layer covers an entire surface of the chip facing the supporting member.

Sub C10

27. (New) A ground plane according to claim 25, wherein:

the dielectric layer covers an entire surface of the chip facing the supporting member.

B1 cont.

28. (New) A ground plane according to claim 24, wherein:

the dielectric layer comprises silicon oxide.

29. (New) A ground plane according to claim 25, wherein:

the dielectric layer comprises silicon oxide.

30. (New) A ground plane according to claim 22, wherein:

the second capacitor plate is a metallic layer on the supporting member.

31. (New) A ground plane according to claim 23, wherein:

the second capacitor plate is a metallic layer on the supporting member.

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32. (New) A ground plane according to claim 23, wherein:

the second capacitor plate is a metallic layer on the supporting member.

33. (New) A ground plane according to claim 23, wherein:

the second capacitor plate is a metallic layer on the supporting member.

34. (New) A ground plane according to claim 23, wherein:

the second capacitor plate is a metallic layer on the supporting member.

35. (New) A ground plane according to claim 23, wherein:

the second capacitor plate is a metallic layer on the supporting member.

36. (New) A ground plane according to claim 23, wherein:

the second capacitor plate is a metallic layer on the supporting member.

37. (New) A ground plane according to claim 23, wherein:

the second capacitor plate is a metallic layer on the supporting member.

38. (New) A ground plane according to claim 30, wherein:

the layer of conductive glue is provided between the metallic layer and the dielectric layer.

39. (New) A ground plane according to claim 31, wherein:

the layer of conductive glue is provided between the metallic layer and the dielectric layer.

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40. (New) A ground plane according to claim 32, wherein:

the layer of conductive glue is provided between the metallic layer and the dielectric layer.

41. (New) A ground plane according to claim 33, wherein:

the layer of conductive glue is provided between the metallic layer and the dielectric layer.

42. (New) A ground plane according to claim 34, wherein:

the layer of conductive glue is provided between the metallic layer and the dielectric layer.

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43. (New) A ground plane according to claim 35, wherein:

the layer of conductive glue is provided between the metallic layer and the dielectric layer.

44. (New) A ground plane according to claim 36, wherein:

the layer of conductive glue is provided between the metallic layer and the dielectric layer.

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45. (New) A ground plane according to claim 37, wherein:

the layer of conductive glue is provided between the metallic layer and the dielectric layer.

46. (New) A ground plane according to claim 22, wherein:

the at least one electrically conducting via extending through the supporting member is directly connected to the second capacitor plate.

47. (New) A ground plane according to claim 30, wherein:

the vias and the metallic layer are integrally formed from a same metal.

48. (New) A method for providing a ground plane for a semiconductor chip mounted on a supporting member in a chip package, comprising providing a metal covered area on the surface of the supporting member, providing vias electrically connected to the metal covered area and extending therefrom through

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the supporting member to the opposite side thereof, connecting in parallel at least two of the vias, and using a conductive glue between the chip and the metal covered area to attach the metal covered area to the chip.

49. (New) A semiconductor chip package comprising:

a semiconductor chip and a supporting member, the supporting member comprising at least one metal covered area and at least one electrically conductive via extending from the metal covered area through the supporting member, wherein the chip is adhered to the supporting member by means of a conductive glue and the conductive glue is in electrical contact with the metal covered area.

REMARKS

The present invention is a ground plane, a method for providing a ground plane, and a semiconductor chip. In accordance with the invention, a ground plane for a semiconductor chip 1 for mounting on a supporting member 4 in a chip package in accordance with the invention includes at least one first capacitor plate within the chip 1, and at least one second capacitor plate 3 which is conductive glue and further serves the purpose of attaching chip 1 to the interposer or lead frame 4. The first and second capacitor plates are separated by dielectric layer 2 which may be silicon dioxide and are capacitively coupled to each other via the dielectric layer 2. The grounding plane comprises at least one first conducting member including at least one electrically conductive via 7